



N-Channel Enhancement-Mode Vertical DMOS FET

Features

- ▶ Low threshold — 1.6V max.
- ▶ High input impedance
- ▶ Low input capacitance — 140pF typical
- ▶ Fast switching speeds
- ▶ Low on-resistance
- ▶ Free from secondary breakdown
- ▶ Low input and output leakage
- ▶ Complementary N- and P-channel devices

Applications

- ▶ Logic level interfaces – ideal for TTL and CMOS
- ▶ Solid state relays
- ▶ Battery operated systems
- ▶ Photo voltaic drives
- ▶ Analog switches
- ▶ General purpose line drivers
- ▶ Telecom switches

Ordering Information

BV _{DSS} /BV _{DGS} (V)	R _{DS(ON)} max (Ω)	I _{D(ON)} min (A)	V _{GS(th)} max (V)	Package Options	
				TO-92	20-Lead SOW
40	0.75	4.0	1.6	TN0604N3-G	-
40	1.0	4.0	1.6	-	TN0604WG-G

-G indicates package is RoHS compliant ('Green')



Absolute Maximum Ratings

Parameter	Value
Drain-to-source voltage	BV _{DSS}
Drain-to-gate voltage	BV _{DGS}
Gate-to-source voltage	±20V
Operating and storage temperature	-55°C to +150°C
Soldering temperature*	300°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

* Distance of 1.6mm from case for 10 seconds.

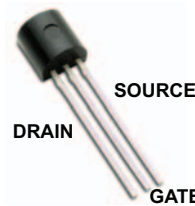
Product Marking



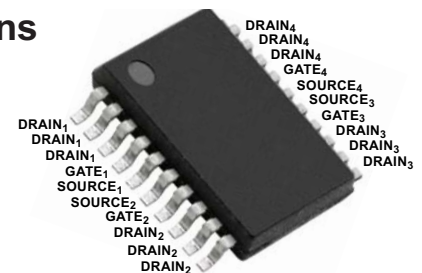
YY = Year Sealed
 WW = Week Sealed
 _____ = "Green" Packaging

TO-92 (N3)

Pin Configurations



TO-92 (N3)



20-Lead SOW (WG)

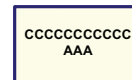
Product Marking

Top Marking



YY = Year Sealed
 WW = Week Sealed
 L = Lot Number
 C = Country of Origin*
 A = Assembler ID*
 _____ = "Green" Packaging

Bottom Marking



*May be part of top marking

20-Lead SOW (WG)

Thermal Characteristics

Package	I _D (continuous) ⁽¹⁾ (A)	I _D (pulsed) (A)	Power Dissipation @T _A = 25°C (W)	θ _{jc} (°C/W)	θ _{ja} (°C/W)	I _{DR} ⁽¹⁾ (A)	I _{DRM} (A)
TO-92 (N3)	0.7	4.6	0.74	125	170	0.7	4.6
20-Lead SOW (WG)	1.0	4.0	1.5	-	84	1.0	4.0

Notes:

(1) I_D (continuous) is limited by max rated T_J.

Electrical Characteristics (@25°C unless otherwise specified)

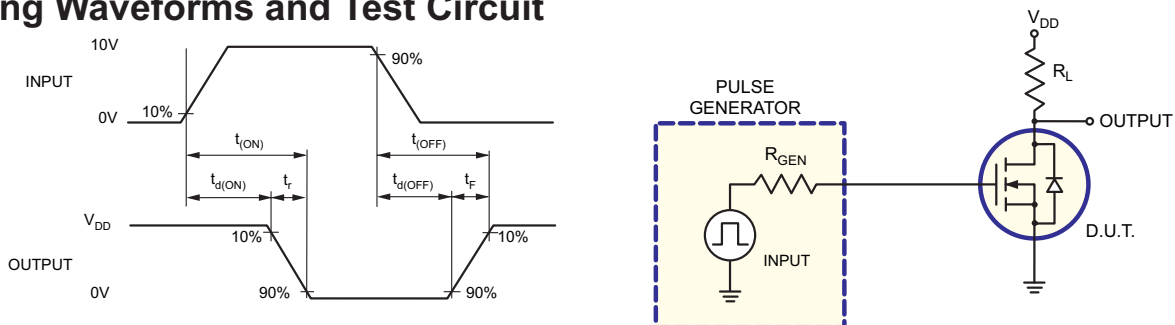
Sym	Parameter	Min	Typ	Max	Units	Conditions	
BV _{DSS}	Drain-to-source breakdown voltage	40	-	-	V	V _{GS} = 0V, I _D = 2.0mA	
V _{GS(th)}	Gate threshold voltage	0.6	-	1.6	V	V _{GS} = V _{DS} , I _D = 1.0mA	
ΔV _{GS(th)}	Change in V _{GS(th)} with temperature	-	-3.8	-4.5	mV/°C	V _{GS} = V _{DS} , I _D = 2.5mA	
I _{GSS}	Gate body leakage	-	-	100	nA	V _{GS} = ± 20V, V _{DS} = 0V	
I _{DSS}	Zero gate voltage drain current	-	-	10	μA	V _{GS} = 0V, V _{DS} = Max Rating	
		-	-	1.0	mA	V _{GS} = 0V, V _{DS} = 0.8 Max Rating, T _A = 125°C	
I _{D(ON)}	ON-state drain current	1.5	2.1	-	A	V _{GS} = 5.0V, V _{DS} = 20V	
		4.0	7.0	-		V _{GS} = 10V, V _{DS} = 20V	
R _{DS(ON)}	Static drain-to-source ON-state resistance	TO-92/ 20-Lead SOW	-	1.0	1.6	Ω	V _{GS} = 5.0V, I _D = 0.75A
		TO-92	-	0.6	0.75		V _{GS} = 10V, I _D = 1.5A
		20-Lead SOW	-	-	1.0		
ΔR _{DS(ON)}	Change in R _{DS(ON)} with temperature	-	0.5	0.75	%/°C	V _{GS} = 10V, I _D = 1.5A	
G _{FS}	Forward transductance	0.5	0.8	-	mmho	V _{DS} = 20V, I _D = 1.5A	
C _{ISS}	Input capacitance	-	140	190	pF	V _{GS} = 0V, V _{DS} = 20V, f = 1.0MHz	
C _{OSS}	Common source output capacitance	-	75	110			
C _{RSS}	Reverse transfer capacitance	-	25	50			
t _{d(ON)}	Turn-ON delay time	-	-	10	ns	V _{DD} = 20V, I _D = 0.5A, R _{GEN} = 25Ω	
t _r	Rise time	-	-	6.0			
t _{d(OFF)}	Turn-OFF delay time	-	-	25			
t _f	Fall time	-	-	20			
V _{SD}	Diode forward voltage drop	-	1.2	1.8	V	V _{GS} = 0V, I _{SD} = 1.5A	
t _{rr}	Reverse recovery time	-	300	-	ns	V _{GS} = 0V, I _{SD} = 1.0A	

Notes:

(1) All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300μs pulse, 2% duty cycle.)

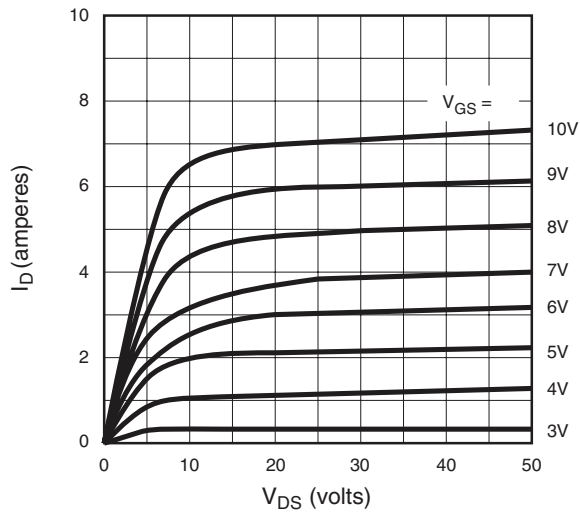
(2) All A.C. parameters sample tested.

Switching Waveforms and Test Circuit

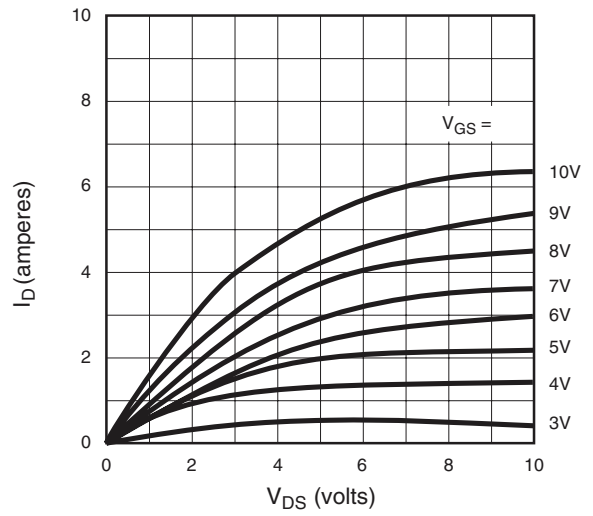


Typical Performance Curves

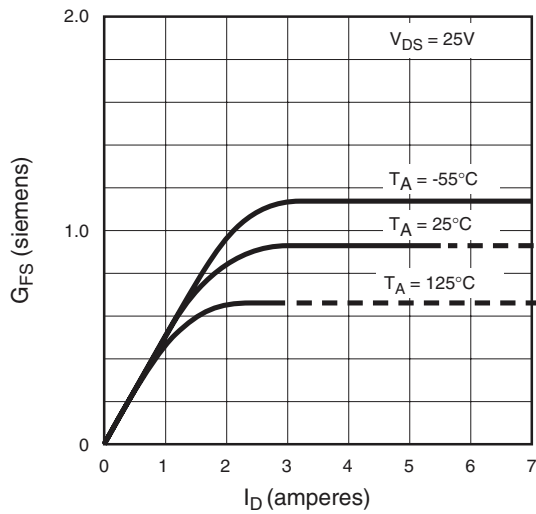
Output Characteristics



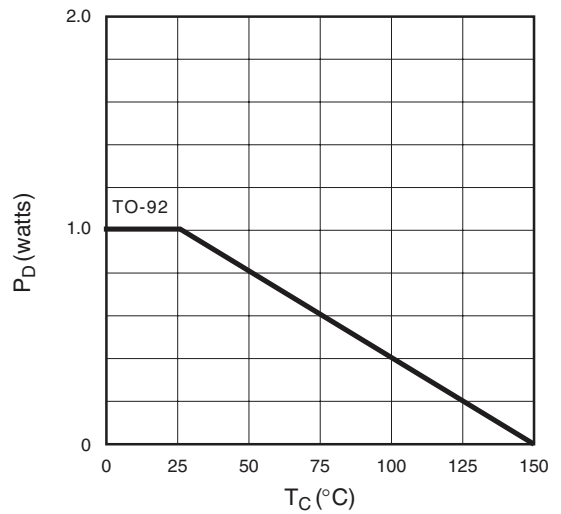
Saturation Characteristics



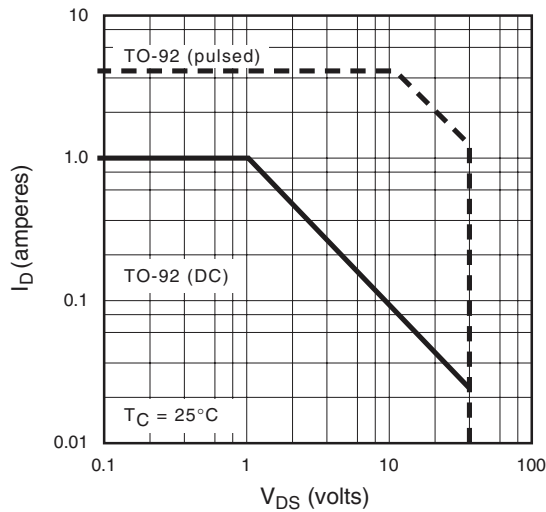
Transconductance vs. Drain Current



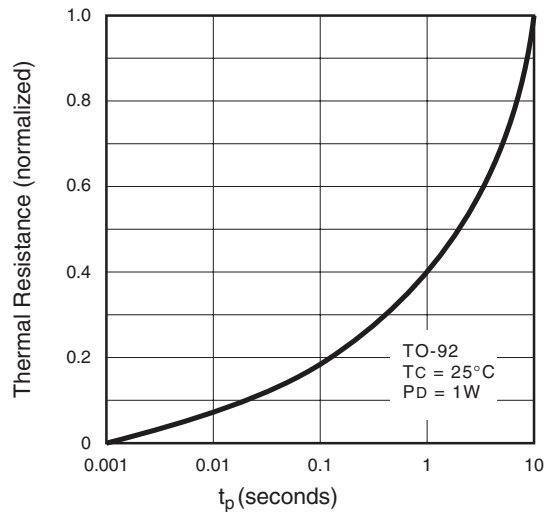
Power Dissipation vs. Case Temperature



Maximum Rated Safe Operating Area

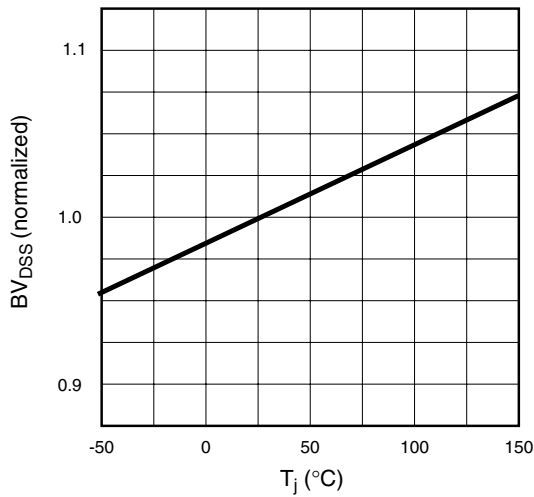


Thermal Response Characteristics

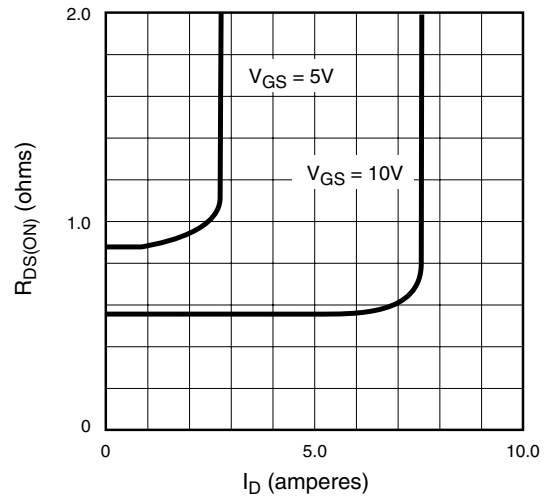


Typical Performance Curves (cont.)

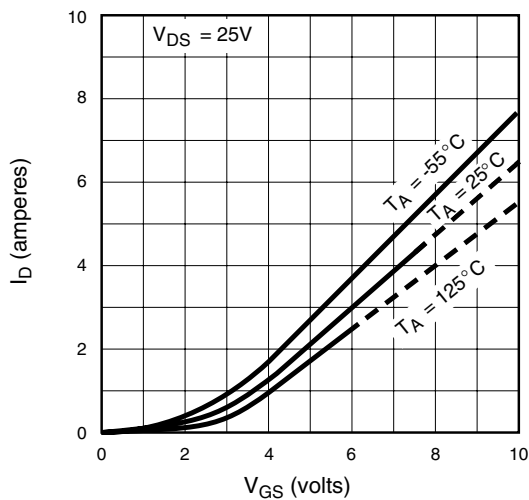
BV_{DSS} Variation with Temperature



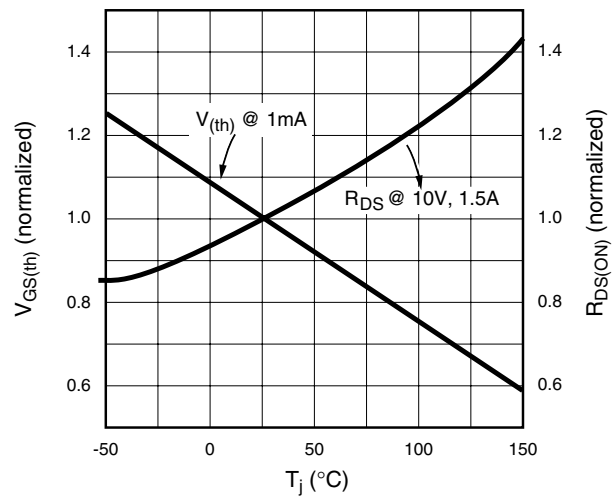
On-Resistance vs. Drain Current



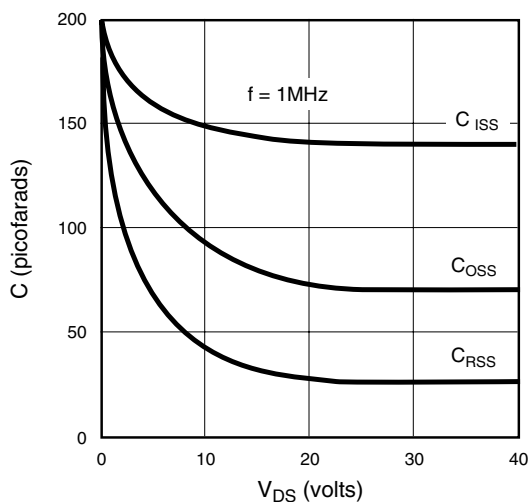
Transfer Characteristics



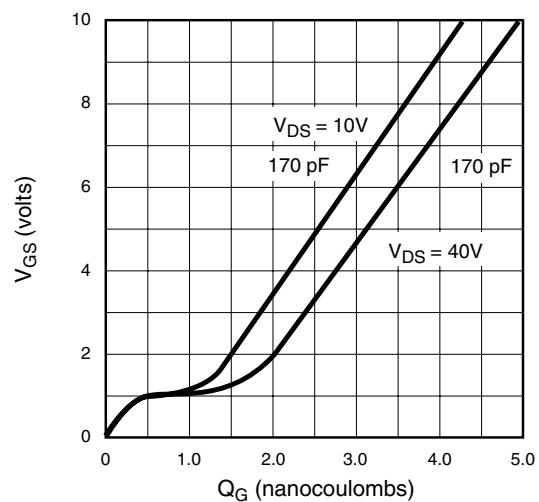
V_(th) and R_{DS} Variation with Temperature



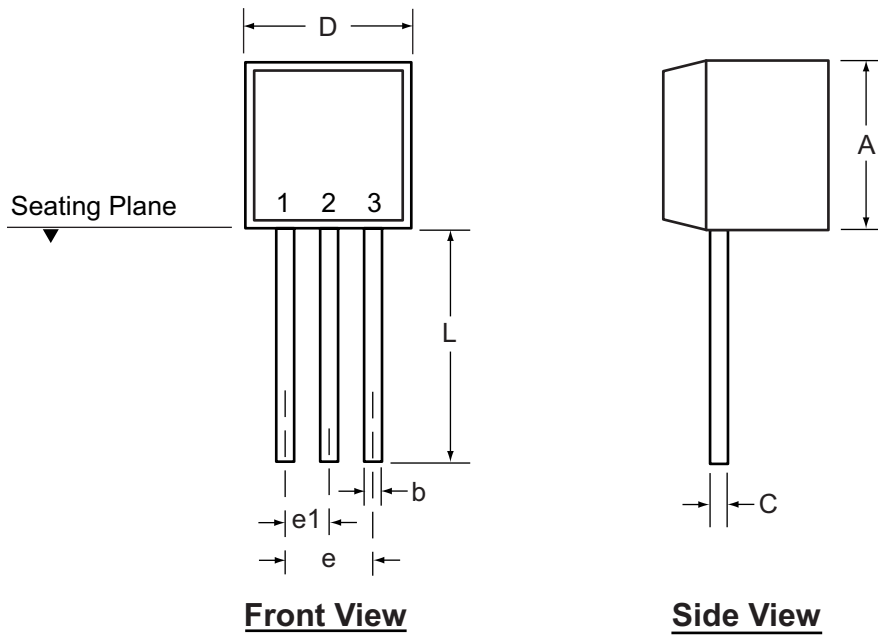
Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



3-Lead TO-92 Package Outline (N3)

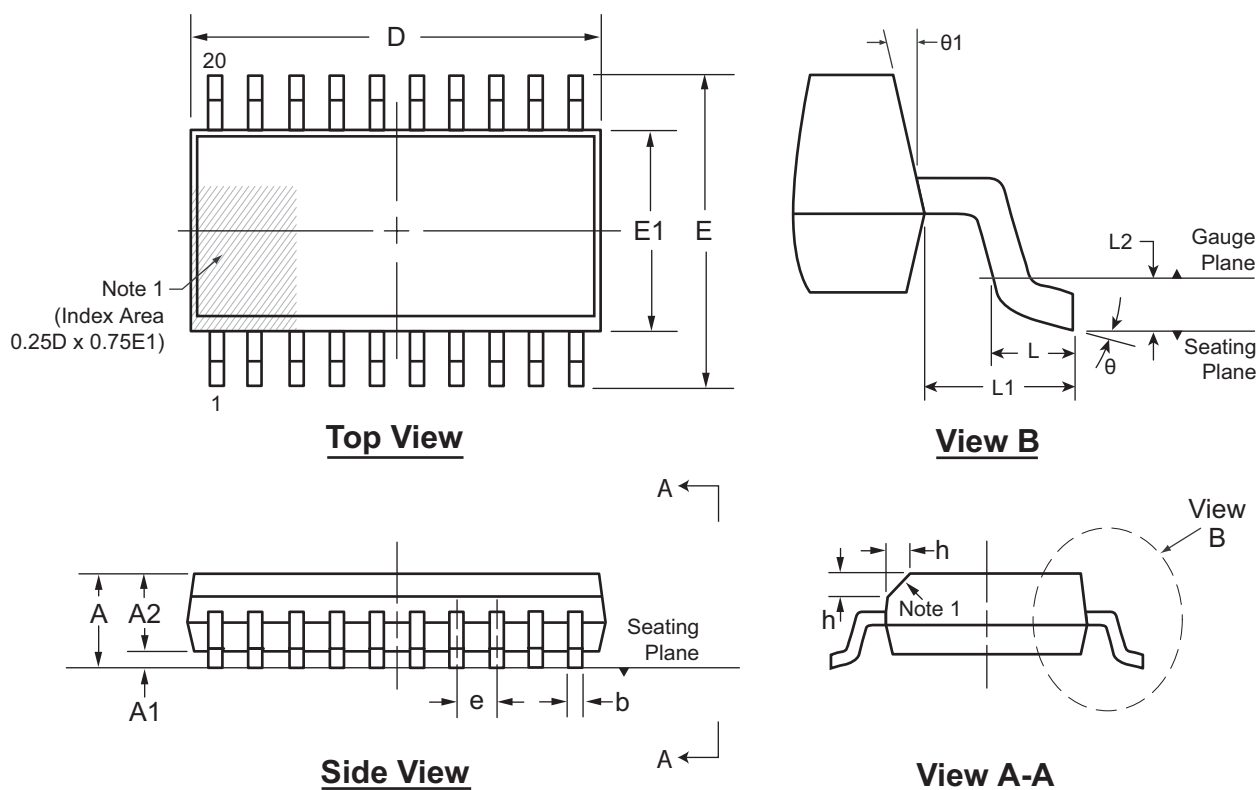


Symbol		A	b	C	D	E	E1	e	e1	L
Dimension (inches)	MIN	.170	.014	.014	.175	.125	.080	.095	.045	.500
	NOM	-	-	-	-	-	-	-	-	-
	MAX	.210	.022	.022	.205	.165	.105	.105	.055	-

Drawings not to scale.

20-Lead SOW (Wide Body) Package Outline (WG)

12.80x7.50mm body, 2.65mm height (max), 1.27mm pitch



Note 1:

This chamfer feature is optional. If it is not present, then a Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier may be either a mold, or an embedded metal or marked feature.

Symbol		A	A1	A2	b	D	E	E1	e	h	L	L1	L2	θ	θ1
Dimension (mm)	MIN	2.15	0.10	2.05	0.31	12.60	9.97	7.40	1.27 BSC	0.25	0.40	1.40 REF	0.25 BSC	0°	5°
	NOM	-	-	-	-	12.80	10.30	7.50		-	-			-	-
	MAX	2.65	0.30	2.55	0.51	13.00	10.63	7.60		0.75	1.27			8°	15°

JEDEC Registration MS-013, Variation AC, Issue E, Sep. 2005.

Drawings not to scale.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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